

In Application Serial No. 10/805,158
Filed May 19, 2004

DECLARATION OF DAVID R. EVANS UNDER 37 CFR §1.132

I, David Russell Evans, Ph.D., hereby declare as follows:

1. My residence address is 7574 S.W. 179th Street, Beaverton, Oregon 97007.
2. Since April 1, 1999 I have been employed by Sharp Laboratories of America, Inc. ("SLA"), 5700 N.W. Pacific Rim Boulevard, Camas, Washington 98607, and between 1993 and April 1, 1999 I was employed by SLA's predecessor company, Sharp Microelectronics Technology, Inc. ("SMT"), located at the same address. My titles at SMT (until April 1, 1999) were, originally, Principal Engineer and, later, Senior Member of the Technical Staff, and my title at SLA, since April 1, 1999, is Senior Manager. My responsibilities include developing advanced process technologies to improve microelectronics fabrication. My technical experience is detailed in the accompanying CV.
3. I have read the claims for the patent application in question, Ono et al., Serial Number 10/805,158 (the Applicant), entitled "Charge Trap Non-Volatile Memory Structure for 2 Bits per Transistor". I have read the Office Action dated March 10, 2006, where claims 16, 17, 20-22, and 25-27 have been rejected as obvious by Halliyal (US 6,451,641), in view of King (US 6,754,104) and Kirkpatrick (US 4,197,144). I have also reviewed the Chooi (US 6,486,080), Agarwal (US 2001/0015453), Liang (US 5,372,957), and Moslehi (US 5,846,883) references cited by the Examiner.
4. The Examiner, on page 4, claims that Halliyal describes all the steps of claim 16, except for the step of inducing trapping centers in a dielectric material. The Examiner further claims that it would have been obvious to one of ordinary skill in the art to induce trapping centers into the dielectric material by exposing the dielectric to an ionized species, as suggested by King and Kirkpatrick, to increase the number of storage sites within the dielectric layer.

5. As explained in the Applicant's specification (pages 1-3), there exist two fundamental non-volatile memory device types: they are floating gate and NROM devices. The floating gate design uses a conductive charge trapping layer, and is not especially relevant to this discussion. The NROM design uses an oxide/nitride/oxide (ONO) structure, interposed between a gate electrode and a FET channel region, where the nitride layer is a non-conductive charge trapping layer. The tradeoff between oxide quality and oxide thickness has encouraged some manufacturers to replace the ONO oxide layers with high-k insulating materials. The Applicant's invention simplifies the problem by replacing the entire ONO structure with a single (non-conductive) high-k dielectric charge trapping layer. Insulating layers are not needed between the Applicant's charge trapping channel and the channel. Neither is an insulator needed between the charge trapping layer and the gate electrode.

6. Halliyal describes a conventional FET made with a high-k dielectric. Halliyal does not describe charge trapping, or the use of a FET as a memory. Halliyal's high-k dielectric cannot store a charge. Halliyal is concerned with depositing polysilicon or silicon-germanium in a manner that does not damage a high-k dielectric. I see no correlation between the Applicant's memory device and Halliyal's FET process.

7. King describes a number of different embodiments that use the combination of a depletion-mode insulated-gate FET (IGFET) and a negative differential resistance (NDR) FET. An IGFET is a conventional FET device. In column 14, King describes the formation of a first electrical insulating layer 1020, with charge traps at or near the interface to the Si substrate 1000. A second (gate) insulator layer 1040 is formed over the first insulator layer 1020, and King describes techniques for forming charge traps in the gate oxide layer (column 14, line 55 through column 15, line 14).

While King does describe the formation of charge traps in an insulator material, such as a high-k dielectric, it is important to understand that these charge trap regions have nothing to do with non-volatility. Rather, King uses his charge traps to create a negative differential resistance (NDR). I see no crossover between NDR and non-volatile memory applications.

8. Kirkpatrick describes a PIN diode device that can be used as a memory because of charge traps formed in the insulator (I) between the PN junction. The insulator is SiO₂, and the trapping sites are formed by implanting Si ions.

9. The Examiner's rationale for combining these three references is not clear to me. Of the three references, only one reference (Kirkpatrick) describes a memory device. Unlike the Applicant's invention, Kirkpatrick describes a diode active device with trapping centers in the SiO₂ insulator between the P and N regions. The Applicant does not describe a SiO₂ insulator, an insulator between P and N regions, or a diode active device. It appears to me that the Examiner could not have found a memory device that is more different from the Applicant's device than Kirkpatrick's.

Of the three primary prior art references presented by the Examiner, the Halliyal and King references seem even more distant from the Applicant's. While the King and Halliyal devices both use a high-k dielectric, neither of these devices can be used for a non-volatile memory. While King describes a high-k dielectric gate oxide with charge trapping centers, King's charge trapping centers cannot hold a charge or store a memory state.


In summary, I can find no apparent reason for an expert in the art to combine three such disparate references as the King, Halliyal, and Kirkpatrick references. Further, I can unequivocally state that this combination does not suggest a memory transistor invention. Even further, the combination of references does not suggest a memory transistor that is able to replace the conventional ONO structure with the high-k dielectric charge trapping region described by the Applicant.

10. In reviewing the other rejections made in view of the Chooi, Agarwal, Liang, and Moslehi references, I note that even if it would have been obvious to add the features cited in these supplemental references, the combination of any or all of these references with Halliyal/King/Kirkpatrick still fails to suggest a device with all the features described in Applicant's claim 16. For example, with respect to claim 28, even if it would have been obvious to use Moslehi's ICP source in combination with Halliyal/King/Kirkpatrick, that combination would not suggest a non-volatile memory transistor made with a high-k gate dielectric, without underlying or overlying oxide layers, where charge trapping centers are formed in the high-k dielectric. Likewise, the

addition of Liang's angled implantation, or Chooi/Agarwal's densification annealing, even when combined with Halliyal/King/Kirkpatrick, does not describe the features of Applicant's claim 16. Therefore, I do not consider these supplemental references particular relevant to the issue of whether the Applicant's invention is obvious.

11. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issuing thereon.

31 July 2006
Date


David R. Evans

David Russell Evans**Professional Education:**

- 1981 Ph. D. in Physical Chemistry, Iowa State University, Ames, Iowa. Dissertation:
"A Comparative Study of Classical and Quantal Approaches to Thermal and
Diffusive Transport in a Dilute Atom-Diatom Binary Mixture"
- 1974 B. S. in Chemistry, Summa Cum Laude, (GPA 3.98) University of Missouri-
Rolla, Rolla, Missouri.

Employment History:

5/1999 - Present

Sr. Manager, Dept. 5, SHARP Laboratories of America, Inc.

Responsible for project management and technical guidance of advanced resistive memory project. Previously, directed CVD copper interconnect research and development. In addition, manage chemical synthesis and associated material development. Directly responsible for advanced CMP research directed toward novel device structures, advanced perovskite materials, noble metals, nanostructures, and sensors.

5/1994 - 5/1999

Sr. Member of Technical Staff, Process Technology Laboratory, SHARP Microelectronics Technology, Inc.

Major responsibility was research and development of chemical mechanical polishing (CMP) of copper for advanced interconnect and dielectric materials for shallow trench isolation and related device structures.

11/1988 - 5/1994

Principal Engineer, Integrated Circuit Operations, Tektronix, Inc.

Major responsibility was thin film development and manufacturing, primarily for use as diffusion barriers and thin film resistors.

11/1986 - 11/1988

Principal Engineer, Liquid Crystal Strategic Program Unit, Tektronix, Inc.

Major responsibility was large area photolithography for optical shutters and passive matrix flat panel displays.

10/1980 - 11/1986

Sr. Development Engineer, Bipolar Process Development Dept., Tektronix, Inc.

Major responsibility was plasma etching and deposition. Implemented the first plasma etch processes for integrated circuit fabrication in Tektronix.

Teaching Experience:

9/1994 - 10/2004

Adjunct Faculty-Oregon Graduate Institute of Oregon Health and Science
University

Graduate level course, Microelectronics Fabrication I, ECE 560, during fall term: The course covers semiconductor materials, crystal structure and growth, thermal oxidation, ion implantation and diffusion. It is part of a one-year sequence in semiconductor processing that typically is taken both by matriculating graduate students from and working professionals drawn from local industry.

3/1981 – 5/1981

Instructor-Iowa State University

Undergraduate level course, Physical Chemistry: The course covered chemical reaction kinetics, kinetic theory of gases, transport theory, x-ray diffraction and crystal structure. Prepared all lectures and exams.

Refereed Journal and Proceedings Publications:

- David R. Evans and Michael R. Oliver, Chemical Mechanical Planarization-Integration Technology and Reliability, Mater. Res. Soc., PV-867, Warrendale, PA, pg. 189, 2005 (invited). "Abrasive Contribution to CMP Friction"
- Parshuram B. Zantye, S. Mudhivarthi, Ashok Kumar, and David Evans, , Chemical Mechanical Planarization-Integration Technology and Reliability, Mater. Res. Soc., PV-867, Warrendale, PA, pg. 75, 2005. "In-situ Metrology for End Point Detection during Chemical Mechanical Polishing of Shallow Trench Isolation Structure"
- Tingkai Li, Sheng Teng Hsu, Bruce Ulrich, and David Evans, *Appl. Phys. Lett.*, 86, 123513, Mar. 18, 2005. "Semiconductive Metal Oxide Ferroelectric Memory Transistor: A Long Retention Non-volatile Memory Transistor"
- T. K. Li, S. T. Hsu, Bruce D. Ulrich, and David R. Evans, *IEEE Trans. on Elec. Dev.*, 50(11), 2280, 2003. "The Thermal Stability of One-Transistor Ferroelectric Memory with Pt-Pb₅Ge₃O₁₁-Ir-Poly-SiO₂-Si Gate Stack"
- T. K. Li, S. T. Hsu, B. Ulrich, L. Stecker, D. Evans, and J. J. Lee, *IEEE Elec. Dev. Lett.*, 23(6), 339, 2002. "One-transistor Ferroelectric Memory with Pt/Pb₅Ge₃O₁₁/Ir/Poly-Si/SiO₂/Si Gate Stack"
- T. K. Li, S. T. Hsu, B. Ulrich, H. Ying, L. Stecker, D. Evans, Y. Ono, J.-S. Maa, and J. J. Lee, *Appl. Phys. Lett.*, 79(11), 1661, 2001. "Fabrication and Characterization of Pb₅Ge₃O₁₁ One-Transistor Memory Device"
- W. Zhuang, L. Charneski, D. Evans, S. T. Hsu, Z. Tang and A. Guloy, *J. de Physique IV, EUROCV D 13*, Aug. 2001. "CVD Copper Thin Film Deposition Using (α -methylstyrene)Cu(I)(hfac)"
- W. Pan, D. Evans, R. Barrowcliff, and S. T. Hsu, *J. de Physique IV, EUROCV D 13*, Aug. 2001. "Growth Kinetics Study of CVD Cu on TiN Barriers"
- F. Zhang, S. T. Hsu, Y. Ono, B. Ulrich, Wei Wei Zhuang, H. Ying, L. Stecker, D. Evans, and J.-S. Maa, *Japan. J. of Appl. Phys.*, 40, L635, 2001. "Fabrication and Characterization of Sub-Micron Pt/Pb₅Ge₃O₁₁/ZrO₂/Si Structure"
- David R. Evans and Michael R. Oliver, Chemical Mechanical Polishing 2001-Advances and Future Challenges, Mater. Res. Soc., PV-671, Warrendale, PA, pg. M1.4.1, 2001 (invited). "Rotational Averaging of Material Removal During CMP"

- David R. Evans, Michael R. Oliver, and Mike Kulus, Chemical Mechanical Planarization IV, Electrochem. Soc. PV-2000-26, Pennington, NJ, pg. 122, 2001. "Morphology Evolution during Copper CMP: Comparison of Fixed Abrasive and Conventional Pads"
- Weiwei Zhuang, Lawrence J. Charneski, David R. Evans, and Sheng Teng Hsu, Advanced Metallization Conference 1999, Mater. Res. Soc., Warrendale, PA, pg. 213, 2000. "New Copper Precursor for Chemical Vapor Deposition of Pure Copper Thin Films"
- Y. Ma, D. R. Evans, T. Nguyen, Y. Ono, and S. T. Hsu, *IEEE Elec. Dev. Lett.*, 20(5), 254, 1999. "Fabrication and Characterization of Sub-Quarter-Micron MOSFET's with a Copper Gate Electrode"
- YanJun Ma, Douglas J. Tweet, Larry Charneski, and David R. Evans, Advanced Metallization Conference in 1998, Mater. Res. Soc., Warrendale, PA, pg. 357, 1999. "Density Oscillation in Sputtered Tantalum Nitride Barrier Metal Thin Films"
- T. Nguyen, L. J. Charneski, and D. R. Evans, *J. of the Electrochem. Soc.*, 144(10), 3634, 1997. "Temperature Dependence of the Morphology of Copper Sputter Deposited on TiN Coated Substrates"
- D. R. Evans, Chemical Mechanical Planarization I, Electrochem. Soc. PV-96-22, Pennington, NJ, pg. 70, 1997. "Electrochemical Interaction between Copper and Barrier Materials During Chemical Mechanical Polishing"
- D. R. Evans, Y. Ono, J.-F. Wang, A. R. Sethuraman, and L. M. Cook, Advanced Metallization and Interconnect Systems for ULSI Applications in 1995, Mater. Res. Soc., Warrendale, PA, pg. 717, 1996. "Yield and Defect Characterization of CMP Copper Metallization"
- Y. Ono, D. R. Evans, and T. Nguyen, Advanced Metallization and Interconnect Systems for ULSI Applications in 1995, Mater. Res. Soc., Warrendale, PA, pg. 165, 1996. "Comparison of Electromigration Characteristics of Pure Copper and Aluminum Alloy Metallizations"
- Z. Karim and D. Evans, Advanced Metallization and Interconnect Systems for ULSI Applications in 1995, Mater. Res. Soc., Warrendale, PA, pg. 101, 1996. "Improvement of the Dielectric Properties of Silsesquioxane Based Spin-on-Polymer by Plasma Treatment and Other Novel Techniques"
- David M. Leet and David R. Evans, *J. of the Electrochem. Soc.*, 142(6), 2013, 1995. "3% Ti-Tungsten Barriers II: The Effect of Deposition Temperature and Nitrogen Inclusion"
- J. Wu, J. D. Parsons, and D. R. Evans, *J. of the Electrochem. Soc.*, 142(2), 669, 1995. "Sulfur Hexafluoride Reactive Ion Etching of (111) β -SiC Epitaxial Layers Grown on (111) TiC Substrates"
- J. Wu, J. D. Parsons, and D. R. Evans, *J. of the Electrochem. Soc.*, 141(10), 2915, 1994. "Reactive Ion Etching of (111) β -SiC Epitaxial Layers on (111) TiC Substrates in $\text{CF}_4 + \text{O}_2 + \text{Ar}$ "
- David M. Leet and David R. Evans, *J. of the Electrochem. Soc.*, 141(7), 1867, 1994. "3% Ti-Tungsten Barriers I: A Discussion of the Role of the A15 Structure"

- D. R. Evans, SOTAPOCS XIII and Metallization of III-V Compound Semiconductors, Electrochem. Soc. PV-91-1, Pennington, NJ, pg. 354, 1991. "Sputter-Deposited Nitrogen-doped Titanium-Tungsten: Material and Etching Characteristics"
- J. Dwire, D. Evans, D. Fuoss, and D. Hoy, SOTAPOCS XIII and Metallization of III-V Compound Semiconductors, Electrochem. Soc. PV-91-1, Pennington, NJ, pg. 346, 1991. "Defect Characterization for a Two-layer Gold I. C. Interconnect"
- D. R. Evans, G. T. Evans, and D. K. Hoffman, *J. of Chem. Phys.*, 93(12), 8816, 1990. "Chattering Collisions and Their Effects on Gas Phase Rotational Energy Relaxation Cross Sections"
- D. J. Economou, D. R. Evans, and R. C. Alkire, *J. of the Electrochem. Soc.*, 135(3), 756, 1988. "A Time Average Model of the RF Plasma Sheath"
- R. G. Cole, D. R. Evans, and D. K. Hoffman, *J. of Chem. Phys.*, 82(4), 2061, 1985. "A Renormalized Theory of Dilute Molecular Gases: Chattering"
- G. T. Evans and D. R. Evans, *J. of Chem. Phys.*, 81(12), 6039, 1984. "Kinetic Theory of Rotational Relaxation in Liquids: Smooth Spherocylinders and Rough Sphere Models"
- D. R. Evans, Plasma Processing IV, Electrochem. Soc. PV-83-10, Pennington, NJ, pg. 199, 1983. "Dry Etched Vias for Two Layer Interconnect on High Density Bipolar Integrated Circuits"
- D. E. Fitz, D. J. Kouri, W.-K. Liu, F. R. McCourt, D. Evans, and D. K. Hoffman, *J. of Phys. Chem.*, 86(7), 1087, 1982. "The Utility of the CS and IOS Approximations for Calculating Generalized Phenomenological Cross Sections in Atom-Diatom Systems"
- V. Khare, D. E. Fitz, D. J. Kouri, D. Evans, and D. K. Hoffman, Potential Energy Surfaces and Dynamics Calculations, ed. D. Truhlar, Plenum, NY, pg. 717, 1981. "On CC and CS Descriptions of Phase Sensitive Cross Sections: Computations for He+HCl"
- D. E. Fitz, D. J. Kouri, D. Evans, and D. K. Hoffman, *J. of Chem. Phys.*, 74(9), 5022, 1981. "On CC, CS, and IOS Generalized Phenomenological Cross Sections for Atom-Diatom Systems"

Conference Presentations:

- John F. Conley, Jr., D. Evans, W. Gao, L. Stecker, and Y. Ono, in collaboration with D. McClain, C. Fei, and J. Jiao, *MRS Meeting-Spring 2005*, San Francisco, CA, Mar. 28-31, 2005. "Self Catalyzed Growth of Nanocones During DC Magnetron Sputtering of an ITO Targets"
- David R. Evans, *MRS Meeting-Spring 2005*, San Francisco, CA, Mar. 28-31, 2005. "Performance of Silicon, Cerium, and Zirconium Oxide Abrasives in Dielectric CMP" (invited)
- Michael R. Oliver and David R. Evans, *MRS Meeting-Spring 2005*, San Francisco, CA, Mar. 28-31, 2005. "Abrasive Contribution to CMP Friction"
- Wei Pan, Robert Barrowcliff, David Evans, and Sheng Teng Hsu, *TMS Annual Meeting-2005*, San Francisco, CA, Feb. 14-16, 2005. "MOCVD Ultra Thin Tungsten Nitride Films as Barrier Metal for Interconnect Applications"

- Tingkai Li, Sheng Teng Hsu, Bruce Ulrich, and David Evans, *MRS Meeting-Fall 2004*, Boston, MA, Nov. 30-Dec. 3, 2004. "Device Structures and Characterization of One Transistor Ferroelectric Memory Devices"
- David R. Evans, *MRS Meeting-Spring 2004*, San Francisco, CA, Apr. 12-16, 2004. "Cerium Oxide – Observations and Analysis" (*invited*)
- T. K. Li, S. T. Hsu, B. Ulrich, and D. Evans, *MRS Meeting-Fall 2003*, Boston, MA, Dec. 1-5, 2003. "Characteristics and Calculation of One-Transistor Memory Devices"
- T. K. Li, B. Ulrich, D. Evans, and S. T. Hsu, *MRS Meeting-Fall 2003*, Boston, MA, Dec. 1-5, 2003. "Selective Deposition of C-Axis Oriented $\text{Pb}_5\text{Ge}_3\text{O}_{11}$ on Patterned Hi-k Gate oxide by MOCVD Processes"
- David R. Evans, *MRS Meeting-Spring 2003*, San Francisco, CA, Apr. 21-25, 2003. "Slurry Admittance and its Effect on Polishing"
- W. Meyer, D. R. Evans, and R. Solanki, *MRS Meeting-Spring 2003*, San Francisco, CA, Apr. 21-25, 2003. "Blech Length versus Titanium-Nitride Barrier Thickness"
- T. K. Li, B. Ulrich, F. Zhang, D. Evans, and S. T. Hsu, *Symp. on Integrated Ferroelectrics*, Colorado Springs, CO, Mar. 9-12, 2003. "The Effects of Integration Processes on the Properties of One Transistor MFMPOS Memory Devices"
- W. W. Zhuang, W. Pan, Sheng Teng Hsu, D. R. Evans, F. Zhang, S. Liu, N. Wu, and A. Ignatiev, *Symp. on Integrated Ferroelectrics*, Colorado Springs, CO, Mar. 9-12, 2003. "Introduction to the Resistance Switch Properties of PCMO Spin-Coating Thin Films"
- David Evans, *2003 CMP for ULSI Multilevel Interconnection Conf. (CMP-MIC)*, Marina Del Ray, CA, Feb. 21, 2003 (*invited*). "Emergent CMP Applications"
- T. K. Li, S. T. Hsu, B. Ulrich, F. Zhang, D. and D. Evans, *MRS Meeting-Fall 2002*, Boston, MA, Dec. 1-5, 2002. "Integration Processes and Properties of One-transistor Memory Devices"
- W. Zhuang, J. Conley, Y. Ono, D. Evans, and R. Solanki, *Int. Joint Conf. on the Applications of Ferroelectrics*, Nara, Japan, May 28-Jun. 1, 2002. "Hafnium Nitrate Precursor Synthesis and Hafnium Oxide Thin Film Properties"
- T. K. Li, S. T. Hsu, B. Ulrich, and D. Evans, *Int. Joint Conf. on the Applications of Ferroelectrics*, Nara, Japan, May 28-Jun. 1, 2002. "Comparison of MFOS and MFMOS One-transistor Memory Devices"
- T. K. Li, S. T. Hsu, B. Ulrich, L. Stecker, and D. Evans, *Int. Joint Conf. on the Applications of Ferroelectrics*, Nara, Japan, May 28-Jun. 1, 2002. "One-transistor Memory Devices with Improved Retention Characteristics"
- David R. Evans, *MRS Meeting-Spring 2002*, San Francisco, CA, Apr. 1-5, 2002 (*invited*). "Comparison and Evolution of Copper CMP Consumable Technology"
- David R. Evans and Michael R. Oliver, *2001 Clarkson Univ. Int. CMP Symp.*, Lake Placid, NY, Aug. 12-15, 2001. "Topological Characteristics of Dielectric Polishing with Ceria Abrasives"
- Fengyan Zhang, Sheng Teng Hsu, Yoshi Ono, Wei Wei Zhuang, Bruce Ulrich, Lisa Stecker, David Evans, and Jer-shen Maa, *13th Int. Symp. on Integrated Ferroelectrics*, Colorado Springs, CO, Mar. 11-14, 2001. "Integration and Characterization of MFI5FET Using $\text{Pb}_5\text{Ge}_3\text{O}_{11}$ "

- David R. Evans, *2000 Clarkson Univ. Int. CMP Symp.*, Lake Placid, NY, Aug. 13-17, 2000. "CMP for Advanced Front End Processing"
- Fengyan Zhang, Sheng Teng Hsu, Hong Ying, David Evans, Shigeo Ohnishi, and Wendong Zhen, *IEEE Int. Symp. on the Applications of Ferroelectrics*, Honolulu, HA, July 31-Aug. 2, 2000. "Integration of SBT Thin Film into MFMOS Structure for One Transistor Memory Applications"
- Douglas Tweet, Sheng Teng Hsu, David R. Evans, Bruce Ulrich, Yoshi Ono, and Lisa Stecker, *ECS Meeting-Spring 2000*, Toronto, ON, Canada, May 14-19, 2000. "High Performance Buried SiGe Channel PMOST Fabricated Using Rapid Thermal Processing and Shallow Trench Isolation"
- Hongning Yang, Douglas Tweet, Lisa Stecker, Wei Pan, David R. Evans, and Sheng Teng Hsu, *ECS Meeting-Spring 2000*, Toronto, ON, Canada, May 14-19, 2000. "Development of PECVD Low- κ Carbon-doped Silicon Oxide Using SiH₄ Based Precursor"
- Hongning Yang, Douglas Tweet, Lisa H. Stecker, David R. Evans, and Sheng Teng Hsu, *MRS Meeting-Spring 2000*, San Francisco, CA, Apr. 24-28, 2000. "Study of SiH₄-based PECVD Low- κ Carbon-doped Silicon Oxide"
- D. R. Evans, M. R. Oliver, and M. K. Ingram, *2000 CMP for ULSI Multilevel Interconnection Conf. (CMP-MIC)*, Santa Clara, CA, Mar. 2-3, 2000. "Separation of Pad and Slurry Effects in Copper CMP"
- David R. Evans, *AVS 1st Int. Conf. on Microelectronics and Interfaces*, Santa Clara, CA, Feb. 9, 2000 (invited). "Electrochemical and Associated Interactions in an Integrated Polished Copper Interconnect Process"
- Yanjuan Ma, Yoshi Ono, Lisa Stecker, David R. Evans, and S. T. Hsu, *IEEE Int. Elec. Dev. Mtg. 1999*, Washington, DC, Dec. 5-8, 1999. "Zirconium Oxide Based Gate Dielectrics with Equivalent Oxide Thickness of Less Than 1.0 nm and Performance of Submicron MOSFET using a Nitride Gate Replacement Process"
- David Evans, Bruce Ulrich, Michael Oliver, and Sharath Hosali, *1999 Clarkson Univ. Int. CMP Symp.*, Lake Placid, NY, Aug. 8-11, 1999. "Polysilicon Polish Stop for STI CMP Using Experimental Slurry"
- David J. Stein, Dale L. Hetherington, James E. Stevens, Michael R. Oliver, Sharath D. Hosali, and David R. Evans, *1999 Clarkson Univ. Int. CMP Symp.*, Lake Placid, NY, Aug. 8-11, 1999. "Oxide CMP Using Ceria-based Slurries"
- S. T. Hsu, D. Evans, T. Nguyen, and H. Yang, *Sixth Symp. on Nano Device Technology*, National Nano Device Laboratories, National Science Council, Taiwan, ROC, May 12-13, 1999. "Cu/a-F:C Interconnect Technology"
- D. R. Evans, *1999 Int. Conf. On GaAs Manufacturing Technology*, Vancouver, BC, Canada, Apr. 19, 1999 (invited). "The Role of CMP in the Fabrication of Advanced Interconnect"
- H. Yang, D. R. Evans, T. Nguyen, L. Stecker, B. Ulrich, and S. T. Hsu, *MRS Meeting-Spring 1999*, San Francisco, CA, Apr. 5-9, 1999. "Multilevel Damascene Interconnection in Integration of MOCVD Cu and Low- κ Fluorinated Amorphous Carbon"

- David J. Stein, Dale L. Hetherington, James E. Stevens, Michael R. Oliver, Sharath D. Hosali, and David R. Evans, *MRS Meeting-Spring 1999*, San Francisco, CA, Apr. 5-9, 1999. "Investigation of a Self-stopping ILD CMP System"
- H. Yang, D. R. Evans, T. Nguyen, L. Stecker, B. Ulrich, and S. T. Hsu, *MRS Meeting-Spring 1999*, San Francisco, CA, Apr. 5-9, 1999. "Multilevel Damascene Interconnection in Integration of MOCVD Cu and Low- κ Fluorinated Amorphous Carbon"
- Tue Nguyen, Hongning Yang, David Evans, Bruce Ulrich, Lisa Stecker, and Sheng Teng Hsu, *1998 Advanced Metallization Conf.*, Colorado Springs, CO, Oct. 6-8, 1998. "Integration of MOCVD Copper and Low- κ Fluorinated Amorphous Carbon in Single and Dual Damascene Interconnection"
- David Evans, *CMP Technology for ULSI Interconnection Seminar at SEMICON West*, San Francisco, CA, Jul. 14, 1998 (invited). "Pattern Dependence and Planarization for Shallow Trench Isolation"
- T. Nguyen, H. Yang, D. R. Evans, and S. T. Hsu, *1998 VLSI Multilevel Interconnection Conf. (VMIC)*, Santa Clara, CA, Jun. 16-18, 1998, pg. 31. "Integration of MOCVD Copper and Low- κ Fluorinated Amorphous Carbon in Single Damascene Structures"
- H. Yang, D. Evans, J. Takason and T. Hara, *ECS Meeting-Spring 1998*, San Diego, CA, May 5, 1998 "Thermal Stability of Organic Interlayers with Low Dielectric Constant"
- Hongning Yang, Douglas Tweet, Yanjun Ma, Tue Nguyen, David Evans, and Sheng Teng Hsu, *MRS Meeting-Spring 1998*, San Francisco, CA, Apr. 13-16 1998. "Thermal Stability and Structural Evolution of Low- κ Fluorinated Amorphous Carbon During Thermal Annealing"
- H. Yang, D. Evans, J. Takason and T. Hara, *Ion Beam Technology Symp.*, Tokyo, Japan, Apr. 1998. "Properties of Organic Low Dielectric Layers"
- David Evans, Bruce Ulrich, and M. Oliver, *1998 CMP for ULSI Multilevel Interconnection Conf. (CMP-MIC)*, Santa Clara, CA, Feb. 16-17, 1998. "Pattern Dependence and Planarization using Silica or Ceria Slurries for Shallow Trench Isolation"
- David Evans, *Int. CMP Symp. at SEMICON Korea*, Seoul, Korea, Jan. 1998 (invited). "Pattern Dependence and Planarization for Shallow Trench Isolation"
- T. Nguyen, Y. Ono, D. R. Evans, Y. Senzaki, M. Kobayashi, L. J. Charneski, B. D. Ulrich, and S. T. Hsu, *ECS Meeting-Fall 1997*, Paris, France, Aug. 31-Sep. 5, 1997. "Electrical Characteristics of CVD Copper Interconnects and Vias"
- D. R. Evans, T. Nguyen, Y. Ono, M. Kobayashi, and S. T. Hsu, *52nd Symp. on Semiconductors and Integrated Circuits Technology*, Japan. ECS, Osaka, Japan, Jun. 12-13, 1997 (invited). "Integration of Copper Metallization with Bulk and SIMOX CMOS Device Technology"
- Tue Nguyen, Dave Evans, and Sheng Teng Hsu, *1997 VLSI Multilevel Interconnection Conf. (VMIC)*, Santa Clara, CA, Jun. 10-12, 1997. "Integration of MOCVD Copper Metallization with SIMOX Devices"
- D. R. Evans, *2nd Int. CMP Symp.*, Tokyo, Japan, Dec. 2, 1996 (invited). "Electrochemical Interaction between Barrier Metals and Copper During Chemical Mechanical Polishing"

- T. Nguyen, B. D. Ulrich, L. R. Allen, and D. R. Evans, *IEEE Symp. on VLSI Technology*, pg. 118, Honolulu, HA, Jun. 11-13, 1996. "A Novel Damascene Process for One Mask Via/Interconnect Formation"
- T. Nguyen, D. Evans, and S. T. Hsu, *ULSI Technology Seminar at SEMICON Kansai*, Osaka, Japan, May 30-31, 1996. "MOCVD Copper Metallization: Deposition and Integration"
- Z. Karim and D. Evans, *1996 Dielectrics for ULSI Multilevel Interconnection Conf. (DUMIC)*, Santa Clara, CA, Feb. 20, 1996. "Integration Issues for Use of Silsesquioxane Based Spin-on-Polymer with Sub-half Micron Technology"
- J-F. Wang, A. R. Sethuraman, L. M. Cook, D. R. Evans, and V. L. Shannon, *1995 VLSI Multilevel Interconnection Conference (VMIC)*, pg. 505, Santa Clara, CA, Jun. 1995. "Chemical Mechanical Polishing of Cu Metallized Multilevel Interconnect Devices"
- T. Nguyen and D. Evans, *MRS Meeting-Fall 1994*, Boston, MA, Nov. 27-Dec. 2, 1994. "Stress and Adhesion of CVD Copper and TiN"
- J.-S. Maa, D. Evans, L. Allen, T. Hsieh, J. Grant, G. Stecker, and B. Ulrich, *SPIE 1994 Microelectronics Manufacturing Conf.*, October 19, 1994. "Monitoring of Highly Selective Plasma Etch Process"

Other Publications:

- D. R. Evans in *Tutorial Session Notes: "Recent Advances in Chemical Mechanical Planarization Technology"*, *MRS Meeting-Spring 2005, San Francisco, CA, Mar. 28-31, 2005*. "CMP Integration"
- D. R. Evans in *Chemical-Mechanical Planarization of Semiconductor Materials* (Springer Series in Materials Science, 69), ed. M. R. Oliver, *Springer-Verlag*, Berlin/Heidelberg, Mar. 2004. "Metal Polishing"
- David Evans, *MRS Bulletin*, 27(10), Oct. 2002, pg. 779. "The Future of CMP"

U. S. Patents Granted:

- T. K. Li, W. W. Zhuang, L. Charneski, D. Evans, and S. T. Hsu, **6,972,239**, Dec. 6, 2005. "Low Temperature MOCVD Processes of $\text{Pr}_x\text{Ca}_{1-x}\text{MnO}_3$ Thin Films"
- T. K. Li, B. Ulrich, D. Evans, and S. T. Hsu, **6,951,825**, Oct. 4, 2005. "Method of Etching SiN/Ir/TaN or SiN/Ir/Ti Stack Using an Aluminum Hard Mask"
- W. W. Zhuang, T. K. Li, D. Evans, S. T. Hsu, and W. Pan, **6,939,724**, Sep. 6, 2005. "Method for Obtaining Reversible Resistance Switches on the PCMO Thin Film Integrated with a Highly Crystallized Seed Layer"
- S. T. Hsu, T. K. Li, and D. Evans, **6,927,120**, Aug. 9, 2005. "Symmetric Crystalline Structure"
- S. T. Hsu, T. K. Li, and D. Evans, **6,927,074**, Aug. 9, 2005. "Asymmetric Memory Cell"
- W. W. Zhuang, D. Evans, and S. T. Hsu, **6,899,858**, May 30, 2005. "Synthesis of Hafnium Nitrate for HfO_2 Thin Film Deposition via ALD Process"
- T. K. Li, W. Pan, R. Barrowcliff, D. Evans, and S. T. Hsu, **6,849,467**, Feb. 1, 2005. "MOCVD of TiO_2 Thin Film for Use as FeRAM H_2 Passivation Layer"

- T. K. Li, S. T. Hsu, D. Evans, and B. Ulrich, 6,794,198, Sep. 21, 2004. "MOCVD Selective Deposition of C-axis Oriented $\text{Pb}_5\text{Ge}_3\text{O}_{11}$ Thin Films on High- κ Gate Oxides"
- W. Pan, J.-S. Maa, D. Evans, and S. T. Hsu, 6,777,327, Aug. 17, 2004. "Barrier Metal Surface Treatment Prior CVD Cu Deposition to Improve Adhesion and Trench Filling"
- F. Zhang, W. W. Zhuang, D. Evans, and S. T. Hsu, 6,774,054, Aug. 10, 2004. "High Temperature Annealing of Spin-on $\text{Pr}_{1-x}\text{Ca}_x\text{MnO}_3$ Thin Film for RRAM Application"
- W. W. Zhuang, L. Charneski, D. Evans, and S. T. Hsu, 6,764,537, Jul. 20, 2004. "Copper Metal Precursor"
- Y. Ma, D. Tweet, and D. Evans, 6,759,695, Jul. 6, 2004. "Integrated Circuit Metal Oxide Semiconductor Transistor"
- W. Pan, D. Evans, and A. Burmaster, 6,723,643, Apr. 20, 2004. "Method for Chemical Mechanical Polishing of Thin Films using End-point Indicator Structures"
- W. Pan, D. Evans, and S. T. Hsu, 6,720,031, Apr. 13, 2004. "Controlling the Initial Growth of CVD Cu Films by Surface Treatment of Barrier Metals"
- W. Pan, D. R. Evans, and S. T. Hsu, 6,716,744, Apr. 6, 2004. "MOCVD of Tungsten Nitride Thin Films Using $\text{W}(\text{CO})_6$ & NH_3 for Cu Barrier Applications"
- D. R. Evans, S. T. Hsu, B. D. Ulrich, D. Tweet, and L. Stecker, 6,716,691, Apr. 6, 2004. "Self-aligned Shallow Trench Isolation Process with Improved Poly Gate Thickness Control"
- W. Zhuang, T. Nguyen, L. Charneski, D. Evans, and S. T. Hsu, 6,669,870, Dec. 30, 2003. "Substituted Phenylethylene Precursor and Synthesis Method"
- W. Pan, W.W. Zhuang, D. Evans, and S. T. Hsu, 6,660,628, Dec. 9, 2003. "MOCVD TiN or TiSiN Barrier Metal Thin Films with Tetrakis(methylethylamino)Titanium (TMEAT) with Octane"
- Y. Ma, D. Evans, Y. Ono, and S. T. Hsu, 6,632,731, Oct. 14, 2003. "Structure and Method of Making a Sub-Micron MOS Transistor"
- D. R. Evans, S. T. Hsu, B. D. Ulrich, D. Tweet, and L. Stecker, 6,627,510, Sep. 30, 2003. "Method of making Self-Aligned Shallow Trench Isolation Process"
- Y. Ma, D. Tweet, and D. R. Evans, 6,620,664, Sep. 16, 2003. "MOSFET with $\text{Si}_{1-x}\text{Ge}_x$ Channel, Deposited Gate Dielectric, and Metal Gate Electrode and Method for Making the Same"
- W. W. Zhuang, L. Charneski, D. Evans, and S. T. Hsu, 6,596,344, Jul. 22, 2003. "Method to Deposit Highly Adhesive Copper Thin Films on Metal Nitride Substrates"
- W.W. Zhuang and D. Evans, 6,586,344, Jul. 1, 2003. "Precursors for Zirconium and Hafnium Oxide Thin Film Deposition"
- W.W. Zhuang, W. Pan, D. Evans, and S. T. Hsu, 6,579,793, Jun. 17, 2003. "Method of Achieving High Adhesion of CVD Copper Thin Films on TaN Substrate"
- W. W. Zhuang, S. T. Hsu, and D. Evans, 6,576,293, Jun. 10, 2003. "Method to Improve the Copper Thin Film Adhesion to Metal Nitride Substrate by the Addition of Water"
- W. W. Zhuang, D. R. Evans, and S. T. Hsu, 6,576,292, Jun. 10, 2003. "Method of Forming Highly Adhesive Copper Thin Films on a Metal Nitride Substrate via CVD"

- Y. Ma, Y. Ono, D. Evans, and S. T. Hsu, 6,573,134, Jun. 3, 2003. "Dual Metal Gate CMOS Devices and Method for Making the Same"
- T. Nguyen, L. Charneski, D. Evans, and S.T. Hsu, 6,555,916, Apr. 29, 2003. "An Integrated Circuit Prepared by Selectively Cleaning Copper Substrates In-Situ, to remove Copper Oxides"
- W. Pan, D. Evans, and S. T. Hsu, 6,509,268, Jan. 21, 2003. "Thermal Densification in the Early Stage of MOCVD Cu for Depositing High Quality Cu Films with Good Adhesion and Trench Filling Characteristics"
- S. T. Hsu and D. Evans, 6,509,260, Jan. 21, 2003. "Method of Shallow Trench Isolation Using a Single Mask"
- S. T. Hsu and D. Evans, 6,506,643, Jan. 14, 2003. "Method for Forming a Damascene FeRAM Cell Structure"
- W. W. Zhuang and D. Evans, 6,472,337, Oct. 29, 2002. "New Precursors for Zirconium & Hafnium Oxide Thin Film Deposition"
- H. Yang, D. R. Evans, and S. T. Hsu, 6,410,462, Jun. 25, 2002. "Method of Making Low- κ Carbon Doped Silicon Oxide"
- S. T. Hsu, D. R. Evans, T. K. Li, J.-S. Maa, and W. W. Zhuang, 6,372,034, Apr. 16, 2002. "PGO Solutions for the Preparation of PGO Thin Films via Spin Coating"
- D. Evans, 6,290,736, Sep. 18, 2001 "Chemically Active Slurry for the Polishing of Noble Metals and Method for Same"
- T. Nguyen, L. Charneski, D. Evans, and S. T. Hsu, 6,281,589, Aug. 28, 2001. "System of Selectively Cleaning Copper Substrate Surfaces, In-Situ, to Remove Copper Oxides"
- W. W. Zhuang, T. Nguyen, L. Charneski, D. Evans, and S. T. Hsu, 6,281,377, Aug. 28, 2001. "Substituted Cycloalkene New Copper Precursors for Chemical Vapor Deposition of Copper Metal Thin Films"
- S. T. Hsu, D. R. Evans, and T. Nguyen, 6,274,421, Aug. 14, 2001. "Method of Making Metal Gate Sub-Micron MOS Transistor"
- W. W. Zhuang, T. Nguyen, L. Charneski, D. Evans, and S. T. Hsu, 6,245,261, Jun. 12, 2001. "Substituted Phenylethylene Precursor and Synthesis Method"
- Y. Ma, D. Tweet, D. Evans and Y. Ono, 6,200,866, Mar. 13, 2001. "Use of Silicon Germanium and Other Alloys as the Replacement Gate for the Fabrication of MOSFETs"
- S. T. Hsu, D. Tweet, W. Pan and D. Evans, 6,194,310, Feb. 27, 2001. "Method of Forming Conductive Diffusion Barriers"
- S. T. Hsu, H. Yang, D. Evans, T. Nguyen, and Y. Ma, 6,184,157, Feb. 6, 2001. "Stress-Loaded Film and Method for Same"
- D. Evans and S. T. Hsu, 6,133,106, Oct. 17, 2000. "Fabrication of a Planar MOSFET with Raised Source/Drain by Chemical Mechanical Polishing and Nitride Replacement"
- W. W. Zhuang, T. Nguyen, R. Barrowcliff, D. Evans, and S. T. Hsu, 6,090,963, Jul. 18, 2000. "Alkene Ligand Precursor and Synthesis Method"
- W. W. Zhuang, T. Nguyen, G. Stecker, D. Evans, and S. T. Hsu, 6,015,918, Jan. 18, 2000. "Allyl-Derived Precursor and Synthesis Method"
- W. W. Zhuang, T. Nguyen, L. Charneski, D. Evans, and S. T. Hsu, 5,994,571, Nov. 30, 1999. "Substituted Ethylene Precursors and Synthesis Method"

- T. Nguyen, L. Charneski, D. Evans, and S. T. Hsu, 5,939,334, Aug. 17, 1999. "System and Method of Selectively Cleaning Copper Substrate Surfaces, in-situ to Remove Copper Oxides"
- T. Nguyen, B. Ulrich, and D. Evans, and S. T. Hsu, 5,936,707, Aug. 10, 1999. "Multi-Level Reticle System and Method for Forming Multi-level Resist Profiles"
- T. Nguyen, B. Ulrich, and D. Evans, and S. T. Hsu, 5,914,202, Jun. 22, 1999. "Multi-Level Reticle System and Method for Forming Multi-level Resist Profiles"
- J. J. Lee, D. R. Evans, and S. T. Hsu, 5,907,762, May 25, 1999. "Method of Manufacture of Single Transistor Ferroelectric Memory Cell Using Chemical Mechanical Polishing"
- T. Nguyen, B. Ulrich, and D. Evans, and S. T. Hsu, 5,906,910, May 25, 1999. "Multi-Level Reticle System and Method for Forming Multi-level Resist Profiles"
- D. R. Evans, J. S. Flores, and S. Dottarar, 4,732,865, Mar. 22, 1988. "Self-aligned Internal Mobile Ion Getter for Multi-layer Metallization on Integrated Circuits"

Continuing Education and Other Skills:

Broad experience related to collaborative research and development efforts with universities, government laboratories, and private companies. This includes writing legally binding contracts and statements of work, administering grants, and managing collaborative efforts of a more informal nature.

Taken several electrical engineering courses through Oregon State University, Portland State University, and University of Portland that cover fundamental circuits and devices. Additionally, have participated in several work-related technical and management training programs.

Proficient in applied mathematics and algorithm construction.